a Si substrate; and

a resistance element formed on said Si substrate,

said resistance element comprising:

a first resistance pattern provided on said substrate at a first level; and

a second resistance pattern provided adjacent to said first resistance pattern at a second level lower than said first level, said second resistance pattern being electrically connected in series to said first resistance pattern to form said resistance element,

said second resistance pattern having an edge defined by said first resistance pattern.

REMARKS

The application has been reviewed in light of the Office Action dated April 1, 2002. Claims 1-8 are pending in this application, with claim 1 being in independent form and claim 8 withdrawn from consideration. By the present Amendment, 1 has been amended. It is submitted that no new matter has been added and no new issues have been raised by the present Amendment.

Claims 1-3, 5, 7 and 8 were also rejected under Section 102(b) as allegedly anticipated by U.S. Patent 4,804,636 to Groover III, et al. Claims 1-8 were rejected under 35 U.S.C. §103(a) as allegedly obvious from U.S. Patent 5,911,114 to Naem. Applicants have carefully considered the Examiner's comments and the cited art, and respectfully submit independent claim 1 is patentably distinct from the cited art, for at least the following reasons.

The present disclosure is directed to semiconductor devices having an integral

resistance element. A second resistance pattern is provided adjacent to a first resistance pattern at a second level lower than the first level of the first resistance pattern, the second resistance pattern being electrically connected in series to the first resistance pattern to form the resistance element and the second resistance pattern having an edge defined by the first resistance pattern. The claimed structure allows for the variation of the total resistance of the resistance elements to be effectively compensated for (page 13, lines 11-22).

Groover, III et al., as understood by Applicants, relates to a process for making integrated circuits having titanium nitride triple interconnect. Groover, III et al. refers to poly layers used for poly-to-poly capacities and/or sometimes resistors. The Office Action refers to gate electrode N1 as an upper resistance pattern and S/D 204 as a lower resistance pattern.

However, Applicant also finds no teaching or suggestion in Groover, III et al. of a substrate and a resistance element formed on the substrate, the resistance element comprising a first resistance pattern provided on the substrate at a first level and a second resistance pattern provided adjacent to the first resistance pattern at a second level lower than the first level, the second resistance pattern being electrically connected in series to the first resistance pattern to form the resistance element, the second resistance pattern having an edge defined by the first resistance pattern, as recited in independent claim 1.

Accordingly, Applicants submit independent claim 1 is patentably distinct from Groover III et al.

Naem, as understood by Applicants relate to a method of simultaneous formation of salicide and local interconnects in an integrated circuit structure. The Office Action indicates

that Naem shows a similar configuration to that shown in Groover III et al.

However, Applicants also find no teaching or suggestion in Naem of a substrate and a resistance element formed on the substrate, the resistance element comprising a first resistance pattern provided on the substrate at a first level and a second resistance pattern provided adjacent to the first resistance pattern at a second level lower than the first level, the second resistance pattern being electrically connected in series to the first resistance pattern to form the resistance element, the second resistance pattern having an edge defined by the first resistance pattern.

Accordingly, Applicants submit independent claim 1 is also patentable over Naem.

The Office is hereby authorized to charge any additional fees that may be required in connection with this amendment and to credit any overpayment to our Deposit Account No. 03-3125.

If a petition for an extension of time is required to make this response timely, this paper should be considered to be such a petition, and the Commissioner is authorized to charge the requisite fees to our Deposit Account No. 03-3125.

If a telephone interview could advance the prosecution of this application, the Examiner is respectfully requested to call the undersigned attorney.

Entry of this amendment and allowance of this application are respectfully requested.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES IN THE CLAIMS

1. (Twice Amended) A semiconductor device, comprising:

a Si substrate; and

a resistance element formed on said Si substrate,

said resistance element comprising:

a first resistance pattern provided on said substrate at a first level; and

a second resistance pattern provided adjacent to said first resistance pattern at a second level lower than said first level, said second resistance pattern being electrically connected in series to said first resistance pattern to form said resistance element,

said second resistance pattern having an edge defined by said first resistance pattern.